# Anode-Shorted Gate Turn-Off Thyristor

## Type G1000L#250

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Voltage Ratings</th>
<th>Maximum Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DRM}$</td>
<td>2500</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RSM}$</td>
<td>2500</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RRM}$</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DC-link}$</td>
<td>1400</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ratings</th>
<th>Maximum Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{TGQM}$</td>
<td>1000</td>
<td>A</td>
</tr>
<tr>
<td>$L_s$</td>
<td>0.3</td>
<td>µH</td>
</tr>
<tr>
<td>$I_{(AVM)}$</td>
<td>500</td>
<td>A</td>
</tr>
<tr>
<td>$I_{(RMS)}$</td>
<td>970</td>
<td>A</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>7.5</td>
<td>kA</td>
</tr>
<tr>
<td>$I_{SM2}$</td>
<td>8.9</td>
<td>kA</td>
</tr>
<tr>
<td>$I_1^2t$</td>
<td>$125 \times 10^3$</td>
<td>A²s</td>
</tr>
<tr>
<td>$di/dt_{cr}$</td>
<td>1000</td>
<td>A/µs</td>
</tr>
<tr>
<td>$P_{FGM}$</td>
<td>160</td>
<td>W</td>
</tr>
<tr>
<td>$P_{RGM}$</td>
<td>8</td>
<td>kW</td>
</tr>
<tr>
<td>$V_{FGM}$</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>$V_{RGM}$</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>80</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>20</td>
<td>µs</td>
</tr>
<tr>
<td>$T_{op}$</td>
<td>-40 to +125</td>
<td>ºC</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>-40 to +150</td>
<td>ºC</td>
</tr>
</tbody>
</table>

**Notes:**

1) $V_{GK} = -2$Volts.
2) $T_f = 125^\circ C$, $V_D = 80\%V_{DM}$, $V_{DM} < V_{DRM}$, $di_G/dt = 200/\mu s$, $C_S = 2\mu F$.
3) Double-side cooled, single phase; 50Hz, 180° half-sinewave.
4) Half-sinewave, $t_f = 2$ms.
5) For $di/dt > 1000A/\mu s$, consult factory.
6) May exceed this value during turn-off avalanche period.
## Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>TEST CONDITIONS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TM}$ Maximum peak on-state voltage.</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>$I_G=2A, I_T=1000A$.</td>
<td>V</td>
</tr>
<tr>
<td>$I_L$ Latching current.</td>
<td>-</td>
<td>10</td>
<td>50</td>
<td>$T_J=25°C$.</td>
<td>A</td>
</tr>
<tr>
<td>$I_H$ Holding current.</td>
<td>-</td>
<td>10</td>
<td>50</td>
<td>$T_J=25°C$.</td>
<td>A</td>
</tr>
<tr>
<td>$dV/dt_{cr}$ Critical rate of rise of off-state voltage.</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>$V_D=80%V_{DRM}, V_{GR}=-2V$.</td>
<td>V/µs</td>
</tr>
<tr>
<td>$I_{PM}$ Peak off state current.</td>
<td>-</td>
<td>30</td>
<td></td>
<td>Rated $V_{DRM}, V_{GR}=-2V$.</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{RM}$ Peak reverse current.</td>
<td>-</td>
<td>50</td>
<td></td>
<td>Rated $V_{RPM}$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{GKM}$ Peak negative gate leakage current.</td>
<td>-</td>
<td>50</td>
<td></td>
<td>$V_{GR}=-16V$.</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{GT}$ Gate trigger voltage.</td>
<td>-</td>
<td>1.2</td>
<td></td>
<td>$T_J=-40°C$.</td>
<td>V</td>
</tr>
<tr>
<td>$I_{GT}$ Gate trigger current.</td>
<td>-</td>
<td>1.0</td>
<td>4.0</td>
<td>$T_J=25°C$.</td>
<td>A</td>
</tr>
<tr>
<td>$t_d$ Delay time.</td>
<td>-</td>
<td>1.0</td>
<td>300</td>
<td>$V_D=50%V_{DRM}, V_{TG}=1000A, I_{GQ}=20A, dI_{GQ}/dt=20A/µs, dI_{GQ}/dt=300A/µs, (10%I_{GQ} to 90%V_D)$.</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{gt}$ Turn-on time.</td>
<td>-</td>
<td>2.0</td>
<td></td>
<td>Conditions as for $t_d$, (10%I_{GQ} to 10%V_D).</td>
<td>µs</td>
</tr>
<tr>
<td>$I_f$ Fall time.</td>
<td>-</td>
<td>1.0</td>
<td></td>
<td>$V_D=50%V_{DRM}, I_{TG}=1000A, C_3=2\mu F, dI_{GQ}/dt=25A/µs, V_{GR}=-16V, (90%I_{TG} to 10%V_D)$.</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{tg}$ Turn-off time.</td>
<td>-</td>
<td>16</td>
<td>19</td>
<td>Conditions as for $t_f$, (10%I_{TG} to 10%I_{TG}).</td>
<td>µs</td>
</tr>
<tr>
<td>$I_{QF}$ Turn-off gate current.</td>
<td>-</td>
<td>280</td>
<td>19</td>
<td>Conditions as for $t_f$.</td>
<td>A</td>
</tr>
<tr>
<td>$Q_{QF}$ Turn-off gate charge.</td>
<td>-</td>
<td>2000</td>
<td>3000</td>
<td>Conditions as for $t_f$.</td>
<td>µC</td>
</tr>
<tr>
<td>$t_{tail}$ Tail time.</td>
<td>-</td>
<td>40</td>
<td>60</td>
<td>Conditions as for $t_f$, (10%I_{TG} to I_{TG}&lt;1A).</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{gw}$ Gate off-time (see note 3).</td>
<td>120</td>
<td>-</td>
<td>0.05</td>
<td>Double side cooled.</td>
<td>K/W</td>
</tr>
<tr>
<td>$R_{thJK}$ Thermal resistance junction to sink.</td>
<td>-</td>
<td>-</td>
<td>0.13</td>
<td>Cathode side cooled.</td>
<td>K/W</td>
</tr>
<tr>
<td>$F$ Mounting force.</td>
<td>10</td>
<td>-</td>
<td>12</td>
<td>(see note 2).</td>
<td>kN</td>
</tr>
<tr>
<td>$W$ Weight</td>
<td>300</td>
<td>-</td>
<td></td>
<td>Housing option LL</td>
<td>g</td>
</tr>
<tr>
<td></td>
<td>170</td>
<td>-</td>
<td></td>
<td>Housing option LM</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1) Unless otherwise indicated $T_J=125°C$.
2) For other clamping forces, consult factory.
3) The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the passage of tail current.

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Notes on ratings and characteristics.

1. Maximum Ratings.

1.1 Off-state voltage ratings.
Unless otherwise indicated, all off-state voltage ratings are given for gate conditions as diagram 1. For other gate conditions see the curves of figure 3. It should be noted that $V_{DRM}$ is the repeatable peak voltage which may be applied to the device and does not relate to a DC operating condition. While not given in the ratings, $V_{DC}$ should ideally be limited to 65% $V_{DRM}$ in this product.

![Diagram 1](image)

1.2 Reverse voltage rating.
All devices in this series have a minimum $V_{RRM}$ of 18 Volts.

1.3 Peak turn-off current.
The figure given in maximum ratings is the highest value for normal operation of the device under conditions given in note 2 of ratings. For other combinations of $I_{TGO}$, $V_D$ and $C_S$ see the curves of figure 8. The curves are effective over the normal operating range of the device and assume a snubber circuit equivalent to that given in diagram 2. If a more complex snubber, such as an Underland circuit, is employed then the equivalent $C_S$ should be used and $L_s<0.3\mu H$ must be ensured for the curves to be applied.

![Diagram 2](image)

1.4 R.M.S and average current.
Measured as for standard thyristor conditions, double side cooled, single phase, 50Hz, 180° half-sinewave. These are included as a guide to compare the alternative types of GTO thyristors available, values cannot be applied to practical applications, as they do not include switching losses.

1.5 Surge rating and $I^2t$.
Ratings are for half-sinewave, peak value against duration is given in the curve of figure 10.

1.6 Snubber loop inductance.
Use of GTO thyristors with snubber loop inductance, $L_s<0.3\mu H$ implies no dangerous $V_s$ voltages (see diagrams 2 & 3) can be applied, provided the other conditions given in note 1.3 are enforced. Alternatively $V_s$ should be limited to 600 Volts to avoid possible device failure.
1.7 Critical rate of rise of on-state current
The value given is the maximum repetitive rating, but does not imply any specific operating condition. The high turn-on losses associated with limit di/dt would not allow for practical duty cycle at this maximum condition. For special pulse applications, such as crowbars and pulse power supplies, a much higher di/dt is possible. Where the device is required to operate with infrequent high current pulses, with natural commutation (i.e. not gate turn-off), then di/dt>5kA/µs is possible. For this type of operation individual specific evaluation is required.

1.8 Gate ratings
The absolute conditions above which the gate may be damaged. It is permitted to allow $V_{GK(AV)}$ during turn-off (see diagram 10) to exceed $V_{RGM}$ which is the implied DC condition.

1.9 Minimum permissible off time.
This time relates specifically to re-firing of device (see also note on gate-off time 2.7). The value given in the ratings applies only to operating conditions of ratings note 2.

1.10 Minimum permissible on-time.
Figure is given for minimum time to allow complete conduction of all the GTO thyristor islands. Where a simple snubber, of the form given in diagram 1. (or any other non-energy recovery type which discharges through the GTO at turn-on) the actual minimum on-time will usually be fixed by the snubber circuit time constant, which must be allowed to fully discharge before the GTO thyristor is turned off. If the anode circuit has di/dt<10A/µs then the minimum on-time should be increased, the actual value will depend upon the di/dt and operating conditions (each case needs to be assessed on an individual basis).
2 Characteristics

2.1 Instantaneous on-state voltage
Measured using a 500µs square pulse, see also the curves of figure 2 for other values of $I_{TM}$.

2.2 Latching and holding current
These are considered to be approximately equal and only the latching current is measured, type test only as outlined below. The test circuit and wave diagrams are given in diagram 4. The anode current is monitored on an oscilloscope while $V_D$ is increased, until the current is seen to flow during the un-gated period between the end of $I_G$ and the application of reverse gate voltage. Test frequency is 100Hz with $I_{GM}$ & $I_G$ as for $t_d$ of characteristic data.

Diagram 4, Latching test circuit and waveforms.

2.3 Critical dv/dt
The gate conditions are the same as for 1.1, this characteristic is for off-state only and does not relate to dv/dt at turn-off. The measurement, type test only, is conducted using the exponential ramp method as shown in diagram 5. It should be noted that GTO thyristors have a poor static dv/dt capability if the gate is open circuit or $R_{GK}$ is high impedance. Typical values: $-\frac{dv}{dt}<100V/\mu s$ for $R_{GK}>10\Omega$.

Diagram 5, Definition of dV/dt.

2.4 Off-state leakage.
For $I_{DRM}$ & $I_{RRM}$ see notes 1.1 & 1.2 for gate leakage $I_{GK}$, the off-state gate circuit is required to sink this leakage and still maintain minimum of −2 Volts. See diagram 6.

Diagram 6.
2.5 Gate trigger characteristics.
These are measured by slowly ramping up the gate current and monitoring the transition of anode current and voltage (see diagram 7). Maximum and typical data of gate trigger current, for the full junction temperature range, is given in the curves of figure 6. Only typical figures are given for gate trigger voltage, however, the curves of figure 1 give the range of gate forward characteristics, for the full allowable junction temperature range. The curves of figures 1 & 4 should be used in conjunction, when considering forward gate drive circuit requirement. The gate drive requirements should always be calculated for lowest junction temperature start-up condition.

![Diagram 7, Gate trigger circuit and waveforms.](image)

2.6 Turn-on characteristics
The basic circuit used for turn-on tests is given in diagram 8. The test is initiated by establishing a circulating current in Tx, resulting in V_D appearing across C_c/L_c. When the test device is fired C_c/L_c discharges through DUT and commutates Tx off, as pulse from C_c/L_c decays the constant current source continues to supply a fixed current to DUT. Changing value of C_c & L_c allows adjustment of t_{TM} and di/dt respectively, V_D and i are also adjustable.

![Diagram 8, Turn-on test circuit.](image)

The definitions of turn-on parameters used in the characteristic data are given in diagram 10 on page 8. The gate circuit conditions I_{GM} & I_G are fully adjustable, I_{GM} duration 10µs.

The data in the curves of figure 5, gives the turn-on losses with snubber discharge, a snubber of the form given in diagram 2 is assumed. Only typical losses are given due to the large number of variables which effect E_{on}. It is unlikely that all negative aspects would appear in any one application, so typical figures can be considered as worst case. Where the turn-on loss is higher than the figure given it will in most cases be compensated by reduced turn-off losses, as variations in processing inversely effect many parameters. For a worst case device, which would also have the lowest turn-off losses, E_{on} would be 1.5x values given in the curves of figure 5. Turn-on losses are measured over the integral period specified below:-

\[ E_{on} = \int_{0}^{10\mu s} iV\,dt \]

The turn-on loss can be sub-divided into two component parts, firstly that associated with t_{gt} and secondly the contribution of the voltage tail. For this series of devices t_{gt} contributes 50% and the voltage tail 50% (These figures are approximate and are influenced by several second order effects). The loss during t_{gt} is greatly affected by gate current and as with turn-on time, it can be reduced by increasing I_{GM}. The turn-on loss associated with the voltage tail is not effected by the gate conditions and can only be reduced by limiting di/dt, where appropriate a turn-on snubber should be used. In applications where the snubber is discharged through the GTO thyristor at turn-on, selection of discharge resistor will effect E_{on}. The curves of figure 5 are given for a snubber as shown in diagram 2, with R=5Ω, this is the lowest recommended value giving the highest E_{on}, higher values will reduce E_{on}. 

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2.7 Turn-off characteristics

The basic circuit used for the turn-off test is given in diagram 9. Prior to the negative gate pulse being applied constant current, equivalent to I_{TGOM}, is established in the DUT. The switch S_x is opened just before DUT is gated off with a reverse gate pulse as specified in the characteristic/data curves. After the period t_{tg}, voltage rises across the DUT, dv/dt being limited by the snubber circuit. Voltage will continue to rise across DUT until D_c turns-on at a voltage set by the active clamp C_c, the voltage will be held at this value until energy stored in L_x is depleted, after which it will fall to V_{DC}. The value of L_x is selected to give required V_D Over the full tail time period. The overshoot voltage V_{DM} is derived from L_x and forward voltage characteristic of D_C, typically V_{DM}=1.2V_D to 1.5V_D depending on test settings. The gate is held reverse biased through a low impedance circuit until the tail current is fully extinguished.

Diagram 9, Turn-off test circuit.

The definitions of turn-off parameters used in the characteristic data are given in diagram 10 on page 8.
Diagram 10, Turn-on and turn-off parameter definitions.

In addition to the turn-off figures given in characteristic data, the curves of figure 6 give the relationship of $Q_{OG}$ to turn-off current ($I_{TQG}$) and $dQ_{OG}/dt$. Only typical values of $I_{OG}$ are given due to a great dependence upon the gate circuit impedance, which is a function of gate drive design not the device. The $t_{QG}$ is also, to a lesser extent, affected by circuit impedance and as such the maximum figures given in data assume a good low impedance circuit design. The minimum off time to re-fire the device is distinct from $t_{ger}$, the gate off time given in characteristics. The GTO thyristor may be safely re-triggered when a small amount of tail current is still flowing. In contrast, the gate circuit must remain low impedance until the tail current has fallen to zero or below a level which the higher impedance $V_{GR}$ circuit can sink without being pulled down below $-2$ Volts. If the gate circuit is to be switched to a higher impedance before the tail current has reached zero then the requirements of diagram 11 must be applied.

The figure $t_{ger}$, as given in the characteristic data, is the maximum time required for the tail current to decay to zero. The figure is applicable under all normal operating conditions for the device; provided suitable gate drive is employed. At lower turn-off current, or with special gate drive considerations, this time may be reduced (each case needs to be considered individually). Typical turn-off losses are given in the curves of figure 7, the integration period for the losses is nominally taken to the end of the tail time

$E_{off} = \int_0^{t_{ger}+t_{tail}} i_v dv$

($I_{tail} < 1A$) i.e. :-

Diagram 11.
The curves of figure 7 give the turn-off energy with a fixed value of $V_{DM}$ and $V_D=50\%V_{DRM}$. The curves are for energy against turn-off current/snubber capacitance with a correction for voltage inset as an additional graph (snubber equivalent to diagram 2 is assumed). From these curves a typical value of turn-off energy for any combination of $I_{TGO}/C_s$ and $V_D$ or $V_{DM}$ can be derived. Only typical data is included, to allow for the trade-off with on-state voltage ($V_{TM}$) which is a feature of these devices, see diagram 12. When calculating losses in an application, the use of a maximum $V_{TM}$ and typical $E_{off}$ will (under normal operating frequencies) give a more realistic value. The lowest $V_{TM}$ device of this type would have a maximum turn-off energy of 1.5x the figure given in the curves of figures 7.

![Diagram 13](image)

Diagram 12

2.8 Safe turn-off periphery
The necessity to control $dv/dt$ at turn-off for the GTO thyristor implies a trade-off between $I_{TGO}/V_{DM}/C_s$. This information is given in the curves of figure 8. The information in these curves should be considered as maximum limits and not implied operating conditions, some margin of 'safety' is advised with the conditions of the curves reserved for occasional excursions. It should be noted that these curves are derived at maximum junction temperature, however, they may be applied across the full operating temperature range of the device provided additional precautions are taken. At very low temperature, (below $-10^\circ C$) the fall-time of device becomes very rapid and can give rise to very high turn-off voltage spikes, as such it is advisable to reduce snubber loop inductance to <0.2µH to minimise this effect.
Curves

Figure 1 – Forward gate characteristics

- Instantaneous forward gate voltage, \( V_{FG} \) (V)
- Instantaneous forward gate current, \( I_{FG} \) (A)

Minimum and Maximum

For \( T_j = -40°C \) to 125°C

Figure 2 – On-state characteristics of Limit device

- Instantaneous on-state voltage, \( V_T \) (V)
- Instantaneous on-state current, \( I_T \) (A)

\( T_j = 25°C \) and \( T_j = 125°C \)

Figure 3 – Typical forward blocking voltage Vs. external gate-cathode resistance

- External gate-cathode resistance, \( R_{GK} \)
- Forward blocking as a ratio of \( V_{DRM} \)

\( T_j = 125°C \)

Figure 4 – Gate trigger current

- D.C. gate trigger current, \( I_{GT} \) (A)
- Junction temperature, \( T_j \) (°C)

\( T_j = -50°C \) to 150°C
Figure 5 – Typical turn-on energy per pulse (including snubber discharge)

Figure 6 – Maximum gate turn-off charge

Figure 7 – Typical turn-off energy per pulse

Figure 8 – Maximum permissible turn-off current
Figure 9 – Transient thermal impedance

Figure 10 – Maximum $i^2t$ and surge ratings

$T_j$ (initial) = 125°C

$V_{RRM} \leq 10V$

$I_{TSM} \leq 10V$

$I_{TSM} \leq 60\% \times V_{RRM}$

$I^2t: V_{RRM} \leq 10V$

$I^2t: 60\% \times V_{RRM}$

$I_{TSM}: \frac{V_{RRM}}{10V}$

$I_{TSM}: 60\% \times V_{RRM}$

Double side cooled

Anode-Shorted Gate Turn-Off Thyristor type G1000L#250
Outline Drawing & Ordering Information

Outline Option LL

Outline Option LM

ORDERING INFORMATION

(Please quote 10 digit code as below)

<table>
<thead>
<tr>
<th>G1000</th>
<th>L#</th>
<th>Fixed Code</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LL</td>
<td>VDRM/100 25</td>
</tr>
<tr>
<td></td>
<td>LM</td>
<td>VDRM/100 25</td>
</tr>
</tbody>
</table>

Typical order code: G1000LL250 – 2500V VDRM, 26mm clamp height capsule.